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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,918	10/30/2003	Robert S. Vinson	GCSD-1157 (51231-DIV)	8239

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,918	VINSON ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,12-18,28,30 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,12-18,28,30 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10,12-16, 18, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Spielberger et al (U.S. 6,005,778).

As to claim 10, Spielberger et al discloses in figure 6 an integrated circuit chip module comprising: a substrate (as indicated at 14 in figure 1, or 14b in figure 5); an integrated circuit die ("chip" 40c) mounted on the substrate and having die pads (which are connected to wire bonds 90 on chip 40c) and an exposed surface opposite from the substrate; a plurality of substrate bonding pads (18c, 19c) positioned on the substrate adjacent the integrated circuit die ("chip" 40c); and a plurality of decoupling capacitor assemblies (70) mounted on the integrated circuit die ("chip" 40c), each decoupling capacitor assembly comprising: a capacitor carrier (first and second portions of "spacer" 50b) (as indicated in figure 5) secured onto the exposed surface of the integrated circuit die ("chip" 40c), a decoupling capacitor (70) carried by the capacitor carrier; a thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) positioned on the capacitor carrier ("spacer" 50b) (as indicated in figure 5); and a conductive adhesive layer (90) (col. 5, lines 6-7) engaging the decoupling capacitor (70) and thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) and securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5); a wire bond extending from the thin film

metallization layer ("metal layer" 86) (col. 5, lines 8-9) to a logic pin (a logic pin is a bonding pad on chip 40c) of the integrated circuit die ("chip" 40c) and from a logic pin to a substrate bonding pad (18c).

As to claim 12, Spielberger et al discloses in figure 6 an integrated circuit chip module, wherein the plurality of decoupling capacitors (70) are mounted in series along the integrated circuit die (40c).

As to claim 13, Spielberger et al discloses in figure 6 an integrated circuit chip module further comprising: an adhesive (90) (col. 5, lines 6-7) securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5).

As to claim 14, Spielberger et al discloses in figure 6 an integrated circuit chip module further comprising: an adhesive ("electrically conductive adhesive") securing the decoupling capacitor assembly (spacer 50 as indicated in figure 4) to the integrated circuit die (40c or 40a in figure 4) (col. 4, lines 5-30).

As to claim 15, Spielberger et al discloses in figure 6 an integrated circuit chip module, wherein the capacitor carrier ("spacer" 50b) (as indicated in figure 5) is formed from an aluminum nitride substrate ("aluminum nitride") (col. 4, lines 5-16; and col. 6, lines 50-53).

As to claim 16, Spielberger et al discloses in figure 6 an integrated circuit chip module, wherein the aluminum nitride substrate ranges in thickness from about 5 mil to about 50 mil ("approximately 40 mils") (col. 2, lines 65-67).

As to claim 18, Spielberger et al discloses in figure 6 an integrated circuit chip module including: a bonding pad ("dielectric material layer" 84) (col. 4, line 66 – col. 5, line 3) on the thin film metallization layer ("thin metal layer or film" 86) for securing a wire bond.

As to claim 38, Spielberger et al discloses in figure 6 an integrated circuit chip module comprising: a substrate (as indicated at 14 in figure 1, or 14b in figure 5); an integrated circuit die ("chip" 40c) mounted on the substrate and having die pads (which are connected to wire bonds 90 on chip 40c) and an exposed surface opposite from the substrate; a plurality of substrate bonding pads (18c, 19c) positioned on the substrate adjacent the integrated circuit die ("chip" 40c); and a plurality of decoupling capacitor assemblies (70) mounted on each integrated circuit die ("chip" 40c), each decoupling capacitor assembly comprising a capacitor carrier ("spacer" 50b) (as indicated in figure 5) secured onto the exposed surface of the integrated circuit die ("chip" 40c), and a decoupling capacitor (70) carried by the capacitor carrier ("spacer" 50b) (as indicated in figure 5); a wire bond extending from the decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) to a die pad (a die pad is a pad on chip 40c) and from a die pad to a substrate bonding pad (18c); and a wire bond extending from the capacitor carrier ("spacer" 50b) (as indicated in figure 5) to a logic pin (a logic pin is a pad on chip 40c) of said integrated circuit die (chip 40c).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger et al (U.S. 6,005,778) in view Heinks et al (U.S. 5,140,496).

As to claim 17, Spielberger et al does not disclose a wire bond extends from the decoupling capacitor to a logic pin of integrated circuit die.

Spielberger et al does not disclose a wire bond extends from the decoupling capacitor to a logic pin of an integrated circuit die.

Heinks et al discloses in figure 6 a decoupling capacitor assembly, wherein a wire bond (64 or 66) extends from the decoupling capacitor (46) to a logic pin (58 or 60) of an integrated circuit die ("microchip" 12''). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the decoupling capacitor assembly of Spielberger et al by having a wire bond extends from the decoupling capacitor to a logic pin of an integrated circuit die as taught by Heinks et al for electrically connecting the decoupling capacitor to the power supply of the integrated circuit die (see col. 3, lines 7-26).

As to claim 28, Spielberger et al discloses in figure 6 a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) used for decoupling integrated circuit die ("chip" 40c) comprising: a capacitor carrier ("spacer" 50b) (as indicated in figure 5) formed as an aluminum nitride substrate ("aluminum nitride") (col. 4, lines 5-16; and col. 6, lines 50-53) that is about 5 mil to about 50 mil thickness ("approximately 40 mils") (col. 2, lines 65-67); a decoupling capacitor (70) carried by the capacitor carrier ("spacer" 50b) (as indicated in figure 5); an adhesive (90) (col. 5, lines 6-7) securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5); and a thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) formed on the capacitor carrier ("spacer" 50b) (as indicated in figure 5), wherein the adhesive (90) comprises a conductive adhesive (col. 5, line 6)

for conducting current between the capacitor and the capacitor carrier (see col. 5, line 6; and col. 4, lines 40-44).

Spielberger et al does not disclose a wire bond extending from the decoupling capacitor and adapted to be connected to a logic pin of an integrated circuit die.

Heinks et al discloses in figure 6 a decoupling capacitor assembly, wherein a wire bond (64 or 66) extending from the decoupling capacitor (46) and adapted to be connected to a logic pin (58 or 60) of an integrated circuit die ("microchip" 12'). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the decoupling capacitor assembly of Spielberger et al by having a wire bond extending from the decoupling capacitor and adapted to be connected to a logic pin of an integrated circuit die as taught by Heinks et al for electrically connecting the decoupling capacitor to the power supply of the integrated circuit die (see col. 3, lines 7-26).

As to claim 30, Spielberger et al discloses in figure 6 a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) used for decoupling integrated circuit die ("chip" 40c) further comprising: a bonding pad ("dielectric material layer" 84) (col. 4, line 66 – col. 5, line 3) positioned on said capacitor carrier ("spacer" 50b) (as indicated in figure 5) for connecting the wire bond thereto.

Response to Arguments

5. Applicant's arguments with respect to claims 10, 17, 28 and 38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

ZANDRA V. SMITH
PRIMARY EXAMINER
27 Dec 2005